ferroelectric capacitors each having first and second terminals, the first terminal coupled to a drain of a corresponding transistor of the enhancement mode transistors and the second terminal coupled to a common cell plate, for storing data.

**REMARKS**

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1 and 5 have been amended. Claims 1-9 are pending in this application.

The disclosure stands objected to because of the informalities. In response, Applicant has amended the disclosure. Withdrawal of the objection is respectfully requested.

Claims 1, 4 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Hayt. Applicant traverses the rejection for the following reasons.

Applicant submits that Yeh and Hayt, as combined, fail to disclose or suggest a word line coupled to a gate of the depletion mode transistor and a gate of the enhancement mode transistor of claim 1. In other words, the word line is commonly coupled to the gates of the depletion mode transistor and the enhancement mode transistor. In contrast, according to Yeh, a

control potential $V_{WL}$ is applied to the enhancement mode transistor 38 and a floating gate potential $V_{FG}$ is applied to the depletion mode transistor 44. That is, different potentials are applied to the transistors 38 and 44. Applicant submits that Yeh fails to disclose or suggest the word line of claim 1.

Furthermore, Yeh fails to disclose or teach a second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor of claim 1. After a careful review of Yeh, Applicant cannot find any description or drawings which describe the second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor. The Examiner is invited to point out any passages in Yeh which describe or teach the second active area of claim 1.

It is submitted that Hayt does not supply the above-noted deficiencies of Yeh.

Therefore, claim 1 and its dependent claim 4 are not made obvious over Yeh in view of Hayt under 35 U.S.C. §103(a).

With respect to claim 8, Applicant submits that it is improper that claim 8, which is dependent on claim 5 that is not rejected, is included in this rejection.

Claims 2, 3, 5-7 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Hayt, and

further in view of Hoffman. Applicant traverses the rejection for the following reasons.

With respect to claims 2 and 3, which are dependent on claim 1, Applicant submits that Hoffman does not supply the above-noted deficiencies of Yeh and Hayt. Accordingly, claims 2 and 3 are patentable for the same reasons as set forth above with respect to claim 1, as well as on their own merits.

Claim 5 is directed to a ferroelectric random access memory device including a plurality of ferroelectric memory cells. In addition to the reasons set forth above with respect to claim 1, Yeh further fails to disclose or suggest the plurality of ferroelectric memory cells. Yeh merely discloses a non-volatile memory cell 10 in the drawings. Moreover, Hoffman does not supply the above-noted deficiencies of Yeh and Hayt. Therefore, the prior art, either alone or in combination, fail to disclose or suggest the second active areas and the word lines of claim 5, as set forth above with respect to claim 1.

Therefore, claim 5 and its dependent claims 6-7 and 9 are not made obvious over Yeh in view of Hayt and Hoffman under 35 U.S.C. §103(a).

All objections and rejections having been addressed, it is respectfully submitted that claims 1-9 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited

to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

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YSH:dj

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the first full paragraph on page 6 as follows:

The present invention provides, but [id] is not limited to, a 16 cell array. For example, it is possible to implement 32, 64 or 128 cell arrays. At this time, a metal contact may be formed every 16 bits or 32 bits for lowering the resistance of the bit line so that the data applied to the bit line is transmitted through the bit line and the metal contact.

IN THE CLAIMS:

Please amend claims 1 and 5 as follows:

1. (Amended) A ferroelectric memory cell for use in a ferroelectric random access memory (FeRAM) device, the ferroelectric memory cell comprising:

a first active area incorporating therein a gate of a depletion mode transistor;

a second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor;

a word line coupled to the gate of the depletion mode transistor and the gate of the enhancement mode transistor; and

a ferroelectric capacitor having first and second terminals, the first terminal coupled to a drain of the enhancement mode transistor and the second terminal coupled to a cell plate, for

storing data.

5. (Amended) A ferroelectric random access memory (FeRAM) device including a plurality of ferroelectric memory cells, comprising:

first active areas incorporating therein gates of depletion mode transistors;

second active areas adjacent to the first active areas incorporating therein gates of enhancement mode transistors;

word lines coupled to the gates of the depletion mode transistors and the gates of the enhancement mode transistors; and

ferroelectric capacitors each having first and second terminals, the first terminal coupled to [drains] a drain of a corresponding transistor of the enhancement mode transistors and the second terminal coupled to a common cell plate, for storing data.